What is claimed is:

1. A method for forming a trench isolation, comprising:
providing a semiconductor substrate with a trench, wherein the semiconductor substrate has a mask layer;
conformably forming a first insulating layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the first insulating layer;
anisotropically etching the first insulating layer to below the level of the semiconductor substrate;
forming a second insulating layer to cover the semiconductor substrate and the trench; and
planarizing the second insulating layer to expose the mask layer.

2. The method for forming a trench isolation as claimed in claim 1, wherein the mask layer is a nitride layer.

3. The method for forming a trench isolation as claimed in claim 1, wherein the first insulating layer is an oxide layer.

4. The method for forming a trench isolation as claimed in claim 3, wherein the first insulating layer is an LPCVD oxide layer.

5. The method for forming a trench isolation as claimed in claim 1, wherein the anisotropic etching is plasma etching or reactive ion etching.

6. The method for forming a trench isolation as claimed in claim 1, wherein the first insulating layer is lower than the semiconductor substrate by at least 300Å after anisotropic etching.

7. The method for forming a trench isolation as claimed in claim 1, wherein the second insulating layer is an oxide layer.

8. The method for forming a trench isolation as claimed in claim 7, wherein the oxide layer is a TEOS oxide layer.

9. The method for forming a trench isolation as claimed in claim 1, wherein the planarizing is chemical mechanical polishing.

10. A method for forming a trench isolation, comprising:
providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with an opening are sequentially formed thereon;
sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a trench using the patterned photoresist layer as a mask;
removing the patterned photoresist layer;
conformably forming an LPCVD oxide layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the LPCVD oxide layer;
anisotropically etching the LPCVD oxide layer to lower its surface below a top surface of the semiconductor substrate by at least 300Å;

forming an insulating layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the insulating layer;

planarizing the insulating layer to expose the mask layer; and

removing the mask layer.

11. The method for forming a trench isolation as claimed in claim 10, wherein the pad layer is an oxide layer.

12. The method for forming a trench isolation as claimed in claim 10, wherein the mask layer is a nitride layer.

13. The method for forming a trench isolation as claimed in claim 10, wherein the aspect ratio of the trench is greater than 6.

14. The method for forming a trench isolation as claimed in claim 10, wherein the anisotropic etching is plasma etching or reactive ion etching.

15. The method for forming a trench isolation as claimed in claim 10, wherein the insulating layer is an oxide layer.

16. The method for forming a trench isolation as claimed in claim 15, wherein the oxide layer is a TEOS oxide layer.

17. The method for forming a trench isolation as claimed in claim 10, wherein the planarizing is a chemical mechanical polishing.

18. A method for forming a trench isolation, comprising:

providing a semiconductor substrate with a trench, wherein the semiconductor substrate has a mask layer;

forming a first insulating layer to cover the semiconductor substrate and the trench;

anisotropically etching the first insulating layer to form a spacer on a sidewall of the trench;

forming a second insulating layer to cover the semiconductor substrate and the trench; and

planarizing the second insulating layer to expose the mask layer.

19. The method for forming a trench isolation as claimed in claim 18, wherein the mask layer is a nitride layer.

20. The method for forming a trench isolation as claimed in claim 18, wherein the first insulating layer is an oxide layer.

21. The method for forming a trench isolation as claimed in claim 20, wherein the first insulating layer is an LPCVD oxide layer.

22. The method for forming a trench isolation as claimed in claim 18, wherein the anisotropic etching is plasma etching or reactive ion etching.

23. The method for forming a trench isolation as claimed in claim 18, wherein the spacer is lower than the semiconductor substrate.

24. The method for forming a trench isolation as claimed in claim 18, wherein the second insulating layer is an oxide layer.

25. The method for forming a trench isolation as claimed in claim 24, wherein the oxide layer is a TEOS oxide layer.

26. The method for forming a trench isolation as claimed in claim 18, wherein the planarizing is chemical mechanical polishing.

27. A method for forming a trench isolation, comprising:

providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with an opening are sequentially formed thereon;

sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a trench using the patterned photoresist layer as a mask;

removing the patterned photoresist layer;

conformably forming an LPCVD oxide layer to cover the semiconductor substrate and the trench;

anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the trench;

forming an insulating layer to cover the semiconductor substrate and the trench;

planarizing the insulating layer to expose the mask layer; and

removing the mask layer.

28. The method for forming a trench isolation as claimed in claim 27, wherein the pad layer is an oxide layer.

29. The method for forming a trench isolation as claimed in claim 27, wherein the mask layer is a nitride layer.

30. The method for forming a trench isolation as claimed in claim 27, wherein the aspect ratio of the trench is greater than 6.

31. The method for forming a trench isolation as claimed in claim 27, wherein the anisotropic etching is plasma etching or reactive ion etching.

32. The method for forming a trench isolation as claimed in claim 27, wherein the spacer is lower than the semiconductor substrate.

33. The method for forming a trench isolation as claimed in claim 27, wherein the insulating layer is an oxide layer.

34. The method for forming a trench isolation as claimed in claim 33, wherein the insulating layer is a TEOS oxide layer.

35. The method for forming a trench isolation as claimed in claim 27, wherein the planarizing is performed by chemical mechanical polishing.

36. A method for forming a trench isolation, comprising:
providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with a first opening and a second opening are sequentially formed thereon;

sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a first trench and a second trench using the patterned photoresist layer as a mask, wherein the aspect ratio of the first trench is greater than 6;

removing the patterned photoresist layer;

conformably forming an LPCVD oxide layer to cover the semiconductor substrate, the first trench, and the second trench, wherein the first trench is filled with the LPCVD oxide layer;

anisotropical etching the LPCVD oxide layer to lower its surface below a top surface of the semiconductor substrate by at least 300Å;

forming an insulating layer to cover the semiconductor substrate, the first trench and the second trench, wherein the first trench and the second trench are filled with the insulating layer;

planarizing the insulating layer to expose the mask layer; and

removing the mask layer.

37. The method for forming a trench isolation as claimed in claim 36, wherein the pad layer is an oxide layer.

38. The method for forming a trench isolation as claimed in claim 36, wherein the mask layer is a nitride layer.

39. The method for forming a trench isolation as claimed in claim 36, wherein the anisotropic etching is plasma etching or reactive ion etching.

40. The method for forming a trench isolation as claimed in claim 36, wherein the insulating layer is a TEOS oxide layer.

41. The method for forming a trench isolation as claimed in claim 36, wherein the planarizing is performed by chemical mechanical polishing.

42. A method for forming a trench isolation, comprising:
providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with a first opening and a second opening are sequentially formed thereon;
sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a first trench and a second trench using the patterned photoresist layer as a mask, wherein the aspect ratio of the first trench is greater than 6;
removing the patterned photoresist layer;
conformably forming an LPCVD oxide layer to cover the semiconductor substrate;
anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the first trench;
forming an insulating layer to cover the semiconductor substrate, the first trench and the second trench;
planarizing the insulating layer to expose the mask layer; and
removing the mask layer.

43. The method for forming a trench isolation as claimed in claim 42, wherein the pad layer is an oxide layer.

44. The method for forming a trench isolation as claimed in claim 42, wherein the mask layer is a nitride layer.

45. The method for forming a trench isolation as claimed in claim 42, wherein the anisotropic etching is plasma etching or reactive ion etching.

46. The method for forming a trench isolation as claimed in claim 42, wherein the spacer is lower than the semiconductor substrate.

47. The method for forming a trench isolation as claimed in claim 42, wherein the insulating layer is a TEOS oxide layer.

48. The method for forming a trench isolation as claimed in claim 36, wherein the planarizing is chemical mechanical polishing.